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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,843	11/25/2002	John Chester Malinowski	BUR920010074	9709
21254	7590	09/27/2004	EXAMINER	
MCGINN & GIBB, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action**

Application No.

10/065,843

Applicant(s)

MALINOWSKI ET AL.

Examiner

Julio J. Maldonado

Art Unit

2823

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 September 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

**PERIOD FOR REPLY** [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.  
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on \_\_\_\_\_. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.  
2. ☐ The proposed amendment(s) will not be entered because:  
(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ they raise the issue of new matter (see Note below);  
(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_

3. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
4. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.  
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.  
7. ☐ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:


Claim(s) allowed: \_\_\_\_\_

Claim(s) objected to: \_\_\_\_\_

Claim(s) rejected: 9-15 and 21-23.

Claim(s) withdrawn from consideration: \_\_\_\_\_

8. ☐ The drawing correction filed on \_\_\_\_\_ is a) ☐ approved or b) ☐ disapproved by the Examiner.  
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_.  
10. ☐ Other: \_\_\_\_\_

  
George Fourson  
Primary Examiner

Continuation of 5. does NOT place the application in condition for allowance because: Applicant's arguments filed 09/13/2004 have been fully considered but they are not persuasive.

In reference to the combination of Nishimura et al. and Allman et al., applicants argue, "...Claim 9 (and similarly claim 23) recites at least the features of "forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively; and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer...Figs. 1 and 4-6 of Allman clearly show that the optional dielectric layer 47, which allegedly corresponds to the claimed invention's nitride etch stop layer, provides an etch stop for the via extending to the top plate of the capacitor, does not extend-over-the bottom plate 33..."

In response to this argument, Nishimura et al. (Figs.5A-5E) was relied on a method to form a MIM capacitor teach forming a metal-insulator-metal (MIM) capacitor including a step of depositing a silicon nitride layer (516) above the MIM capacitor; forming an interlayer dielectric (517) on the nitride layer (516); forming a first via (519) and a second via (521) through the interlayer and the nitride layer (516) by an etching process above the patterned second metal plate and the first metal plate, respectively (column 5, line 51 - column 6, line 15), but fail to teach using the nitride layer as an etch stop layer.

Taking this into consideration, Allman et al. (Fig.6) was relied on using a first silicon nitride layer (42) formed on top of a first plate electrode (36, 38, 40), and a second silicon nitride layer (47) formed on top of a second plate electrode (44) as etch stop layer during an etching process, wherein in said etching process both of an interlayer dielectric layer (28) and said nitride layers (42 and 47) will eventually be etched. Furtherstill, Allman et al. teach alternative embodiments where this interlayer dielectric and the nitride layers are either simultaneously or selectively etched (column 8, lines 45 - 67). Therefore, using the selective etching process described in Allman et al. to etch the silicon nitride layer and the interlayer dielectric layer in Nishimura et al. would allow further protection to the underlying layers below the nitride layer of Nishimura et al.

Therefore, it would have been within the scope of one of ordinary skill in the art to combine the teachings of Nishimura et al. and Allman et al. to enable using nitride layer of Nishimura et al. to be performed according to the teachings of Allman et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of using the nitride layer of Nishimura et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Also, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981) *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).